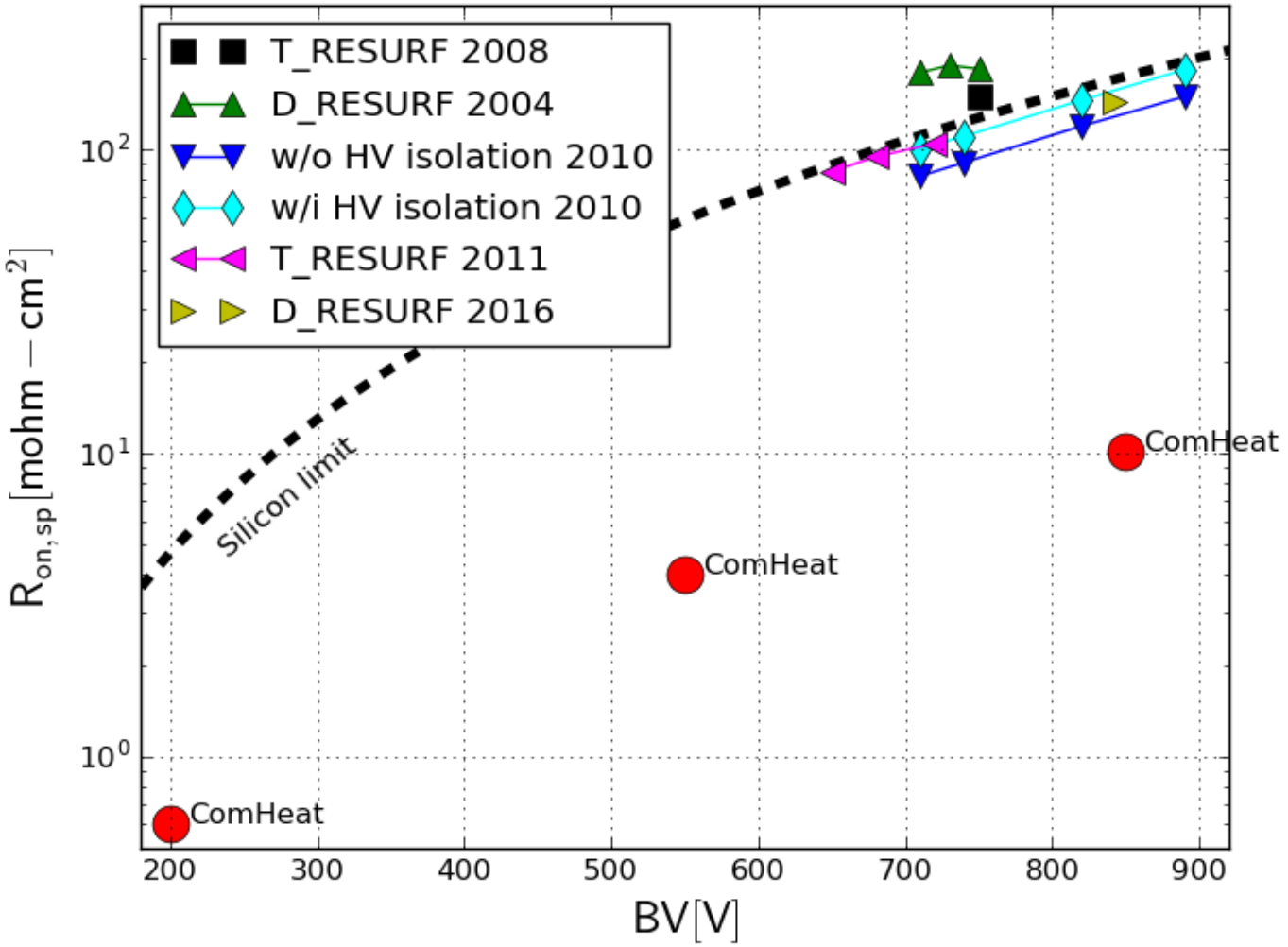
A new LDMOS device concept in combination with CMOS

- Based on existing patents with additional patents on the way.
- Bulk. Breakthrough performance
- TCAD simulations shows very promising performance.
- Voltage range from ~60V to >1000 V.
- At 200V the figure-of-merit $R_{ON}xA$ is 60 mΩmm^2
  - state-of-the-art: 500 mΩmm^2
- In the range 800-900V the $R_{ON}xA$ is 10 mΩcm^2
  - state-of-the-art: 100-150 mΩcm^2

New LDMOS $R_{on,sp}$ vs BV comparison

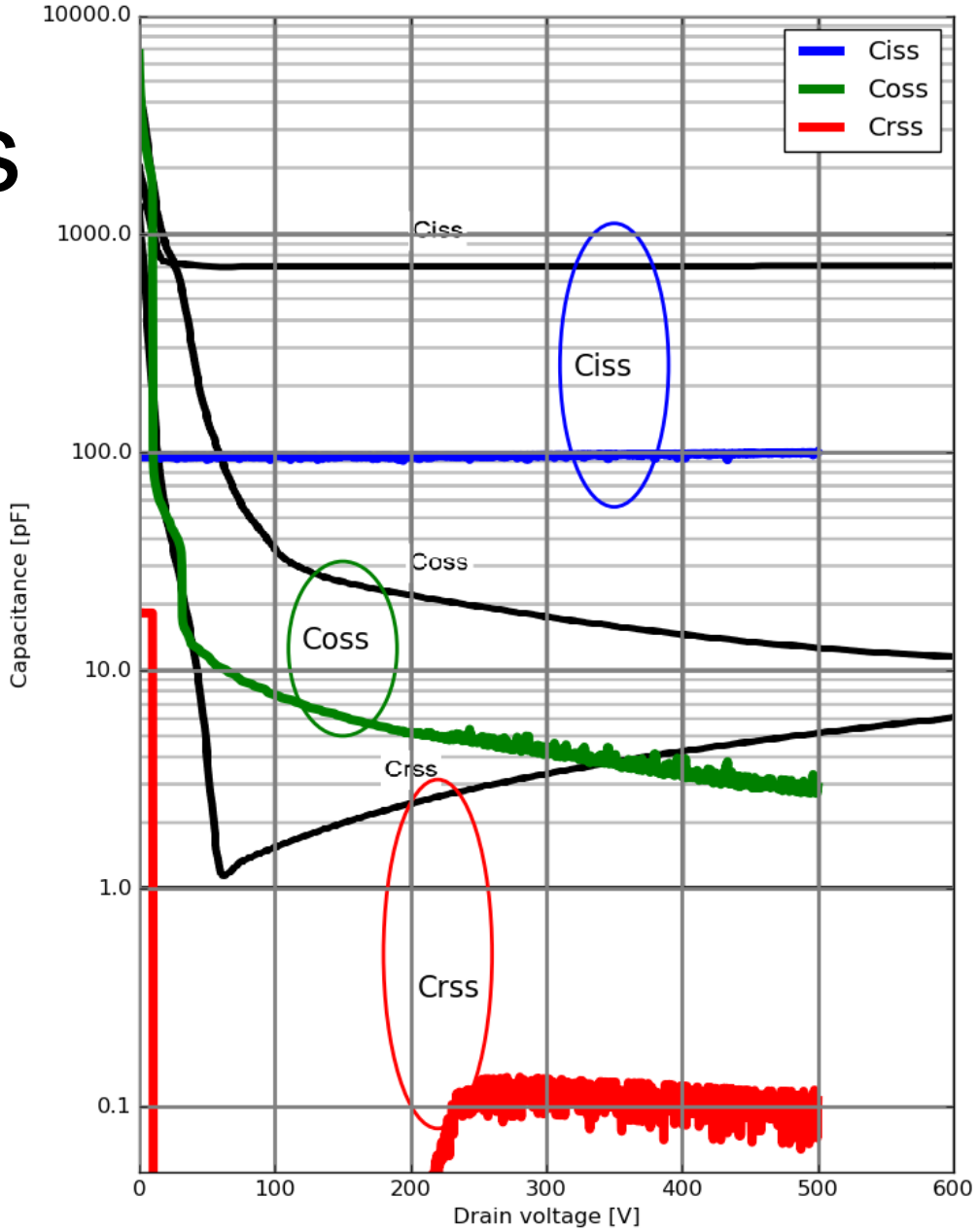


A new LDMOS device concept

- The low figure of merit seems even to be competitive with the best SJ or COOLMOS discrete devices in the 800-900V range.
- This could then be a discrete device where the inherent MOS device can be driven from CMOS logic. No external gate drive circuit.
- To investigate this further we have simulated additional key parameters such as
  - capacitances, max current and transconductance
- Spice models have been developed for the two voltage classes (200V and 800V)

CV-characteristics (simulated)

- Comparison with a discrete device.
- Capacitance for 1ohm devices.
- Black lines is an equivalent device (Infineon IPI90R1K2C3)



CV-characteristics

- The key capacitances are lower for the LDMOS device compared to the discrete device.
  - C_{oss}, 3-4 times lower,
  - C_{iss}, 10 times lower
  - C_{rss}, more than 10 times lower
- They are all very important for overall performance. E.g. switching time is reduced from 40ns down to 4ns (T_{off})
- A low C_{rss} is also very important for protecting for voltage spikes on the drain. Protects the thin gate oxide MOS transistor which also is better shielded from the high voltage from the concept.

Conclusions

- Proposed device can replace a discrete vertical power device with separate gate drive with a one-chip solution controlled directly from CMOS logic (1.5-2V)
  - In the next step logic could be on the same chip, replacing 3 chips with one.
- At 200V e.g. BCD technology, you may have an old LDMOS device which require 5-10 V gate drive in combination with 2V CMOS which then require an additional on-chip power supply. With the new LDMOS device you get rid of the additional power supply and a smaller chip.
- The new devices are compatible with BCD technology both bulk and SOI version.

Conclusions

- So far main focus has been on 200V and 800V with extensive TCAD simulations.
- Regarding figure-of-merit $R_{ON}xA$ we have some preliminary results for 1200V and 1400V with 20 mΩcm² and 27 mΩcm².
- An LIGBT version of the concept has also been preliminary simulated
  - BV = 850 V
  - ~3x more current than to LDMOS at V_{DS}= 4 V.