

A new latch-free LIGBT on SOI or bulk

Lars Vestling and Klas-Håkan Eklund

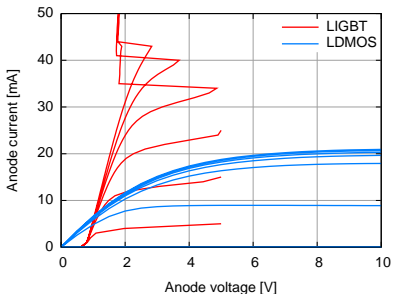
ComHeat Microwave AB
Uppsala, Sweden

2014-03-12

ComHeat Microwave AB is a member of the GigaHertz Centre, Chalmers,
Göteborg, Sweden

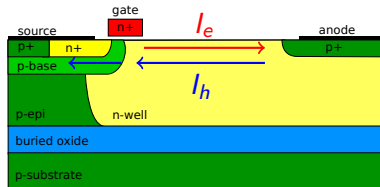
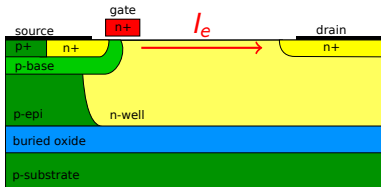
The IGBT

- ▶ Lateral Insulated Gate Bipolar Transistor
- ▶ An IGBT delivers lots of current due to a conductivity modulated drift region.
- ▶ A major problem is the latch-up that limits current and voltage.



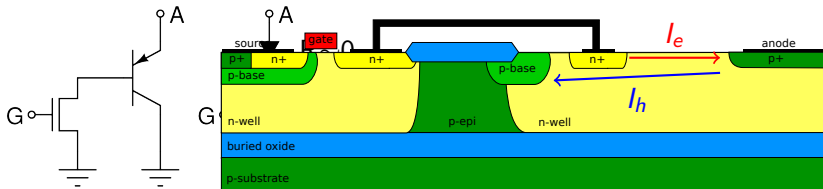
LIGBT and Latch-up

- ▶ Start with an LDMOS transistor.
- ▶ Replace the n+drain with a p+anode.
- ▶ Drift region is now a PNP transistor instead of a resistor.
- ▶ Hole current will increase the body potential and forward bias p-base to source and device gets shortcuted. Latch-up.
- ▶ Can be improved by e.g. lowering the p-base resistance or introduce a hole diverter.



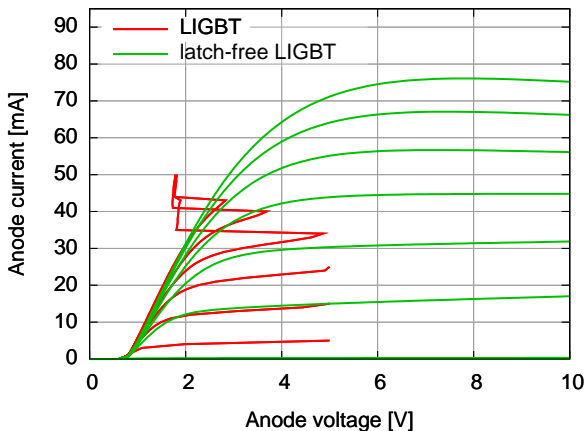
New concept

- ▶ The LIGBT can be represented by a MOSFET in series with a PNP transistor or a PIN diode.
- ▶ The MOS and the PNP are separated electrically/physically.
- ▶ Now the hole current has no chance to reach channel region and latch the device.



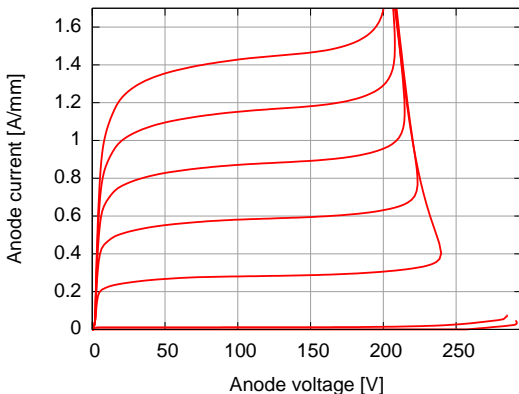
Results

- ▶ Measured IV-characteristics of a basic LIGBT
- ▶ Measured IV-characteristics of the latch-free LIGBT.



No latching

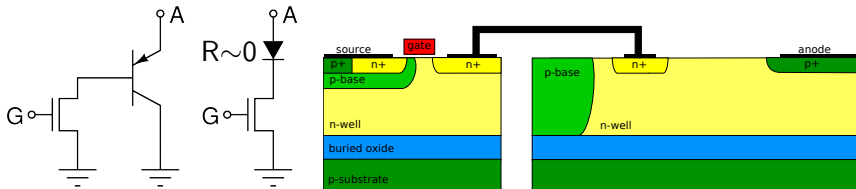
- ▶ Higher current and higher voltage.
- ▶ Faster device ($t_{off} \propto 1/I_{MAX}$)
- ▶ Implementing this device in a 200V SOI foundry technology.



Simulation
results

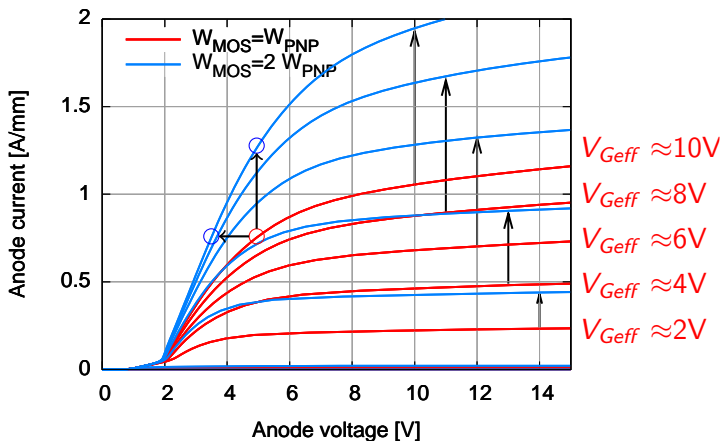
Opportunities

- ▶ The separation of the devices means that it can be done all the way, i.e. two separate devices.
- ▶ The width of the MOS and the width of the PNP (PIN diode) can now be chosen individually.
- ▶ The MOS generates the current. The PNP supports high voltage.
- ▶ On-resistance determined by MOS and not drift region length.



Example: MOSFET wider than PNP (drift region)

$$\blacktriangleright W_{MOS} = 2 \times W_{PNP}$$



Measured results

- ▶ $I_{D,sat} = 1\text{-}2 \text{ A/mm}$ (base width).
 - ▶ state-of-the-art:
 - ▶ SOI-LIGBT (200V): 250 mA/mm
 - ▶ bulk Si-LDMOS (70V): 200 mA/mm,
 - ▶ GaN (70V): 1000 mA/mm
- ▶ Temperature coefficient is 3 times better than LDMOS ($< 350^\circ$)
- ▶ High frequency, $f_T \sim 3 \text{ GHz}$ and $f_{MAX} \sim 10 \text{ GHz}$

Summary

- ▶ New unique IGBT concept demonstrated that totally eliminates latch-up.
- ▶ Drastically improved current capability (2A/mm) in a CMOS compatible technology.
- ▶ Separation of devices gives great flexibility.
 - ▶ Input power reduction
 - ▶ On-resistance reduction
 - ▶ Compatibility with state-of-the-art CMOS (2V).
- ▶ **Remark:** the concept is not tied to any specific technology and can even be used on discrete IGBT devices.

Future work

- ▶ Manufacturing of 200V SOI devices will start March 2014
- ▶ VINNOVA project with Uppsala University and ComHeat Microwave started January 2014 and will study the RF properties of these devices.

Acknowledgements

- ▶ Chalmers for RF-measurements



UPPSALA
UNIVERSITET



CHALMERS